REMARKS

The claims are claims 1 to 12.

The application has been further amended to correct minor errors including the error noted by the Examiner in the paragraph bridging pages 7 and 8 to correct. The application is further amended to update the status of the co-pending application cited on page 1. Lastly, the application has been amended at pages 11 and 17 to conform to the corrected drawings.

Claims are amended in response to the rejections under 35 U.S.C. 112.

Attached are new formal drawings incorporating the changes required by the Examiner. The new formal drawings label Figures 3 to 6 as "PRIOR ART" as required by the Examiner. The label "SYSTCK" of Figure 4 has been changed to "SYSCLK" to match the disclosure in the application at page 11, line 10. Elements 31, 32 and 33 in Figure 4 have been changed to 45, 46 and 47, respectively. Corresponding changes are made in the text application at pages 11 and 17. The arrows on the lines of Figure 4 have been deleted to avoid confusion. Figure 8 has been amended to include signal flow arrows. By these changes it is clear that the MODE signal is an input to switch 202 as taught at page 19, liens 3 to 4.

The Examiner objected to the amendment filed June 20, 2003 under 35 U.S.C. 132 as introducing new matter. The OFFICE ACTION notes at paragraph 4 as new matter: the change "cycles" to "bits" in claims 1 and 4; the "normal mode signal" and "alternative data mode signal" in new claim 6; the "bypass path mode signal" in new claim 8; and the "said start bit generator generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first logic state" and "said output switch

further connecting said serial signal, said start bit and said data..." in new claim 12.

The Applicant respectfully submits that the original application provides disclosure of the recitation of supplying a serial input for a predetermined number of bits. The original application states at page 17, lines 19 to 25:

> "This data transfer protocol includes a first section 121 of plural bits of the same digital state. A second section 130 includes a start bit 131 of the opposite digital state and a predetermined number of data bits 133. Lastly, there is a third section 140 of the first digital state."

Further, the original application cites at page 8, lines 23 to page 9, line 26 a standard known as IEEE 1149.1 or JTAG. In this standard it is known that the signal at the Test Data Input (TDI) is sampled synchronously with the clock signal supplied to the Test Clock input (TCK). Therefore a predetermined number of serial data bits and a predetermined digital level input for the predetermined number of cycles are equivalent. Accordingly, this objection should be withdrawn.

The Applicant respectfully submits that the original application provides disclosure of the mode signals recited in claims 6 and 8. The original application at page 19, lines 3 to 10 recites:

> "Input switch 201 and output switch 202 route the input signal TDI to one of a plurality of paths according to a mode input. The first path is bypass path 203. This bypasses all circuits in the module. The second path is serial scan path 204. Serial scan path 204 is a serial connection of all registers visible via the serial scan path interface in the current module. The third path concerns the alternate data transfer protocol."

This portion of the original specification clearly discloses the three modes recited in claims 6 and 8. The above quoted passage further clearly states that both input switch 201 and output switch 202 select one of the three paths corresponding to a mode input. Claim 6 has been amended to change "normal mode signal" to "serial scan path mode signal" and "alternative data mode signal" to "alternate data transfer protocol mode signal" to correspond more closely to the language used in the application at page 19. This is believed within the scope of the disclosure and more informative than "first mode" and "second mode," which the Applicant submits would be proper. Claim 8 recites "bypass path mode signal" which closely matches the above quoted language. The Applicant respectfully submits that the disclosure that input switch 201 and output switch 202 are responsive to a mode input and disclosure of the respective modes permits the Application to recite corresponding mode names in the claims. Accordingly, this objection should be withdrawn.

The Applicant respectfully submits that the original application provides disclosure of the recitations of claim 12. The application states at page 5, lines 16 to 18:

> "The selected module may transmit return communications via the serial scan path using the same format."

The application includes a similar disclosure at lines 15 and 16 of the original ABSTRACT. The application states at page 19, lines 19 and 19:

> "Example module 200 illustrated in Figure 8 may also transit data via this alternate data transfer protocol."

This "alternative data transfer protocol" is the format illustrated in Figure 7 and described in the original application at page 18,

lines 17 to 30. Thus this "same format" and the "alternative data transfer protocol" disclosed in the above quote portions of the application regarding data transmission by the example module 200 includes the plural bits of the same digital state of first section 121 illustrated in Figure 7. The detailed description of this transmission from example module 200 appearing at page 19, line 18 to page 20, line 2 omits description of portion of the transmission corresponding to first section 121 illustrated in Figure 7. Inclusion of an equivalent of first section 121 is implied from the "same format" language quoted above. Thus the recitation "generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first digital state" of claim 12 is proper. Accordingly, this objection should be withdrawn.

Claims 1 to 12 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not adequately described in the specification. The OFFICE ACTION notes the following inadequately disclosed subject matter: change of "cycles" to "bits" in claims 1 and 4 (paragraph 6-1) noting that "bits" are not necessarily equivalent to "cycles"; the limitation "a predetermined number" in claim 4 (paragraph 6-2); the limitations "normal mode signal", "alternative data mode signal" and "bypass path mode signal" in claims 6 and 8 (paragraph 6-3); the limitations "said start bit generator generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first logic state" and "said output switch further connecting said serial signal, said start bit and said data..." of claim 12 (paragraph 6-4).

The substitution of "bits" for "cycles" is adequately disclosed in the original application. As noted above, this is described in the application at page 18, lines 19 to 24. Further, by teaching that the preferred embodiment employs an known standard

(IEEE 1149.1 also known as JTAG), a predetermined digital level input for the predetermined number of cycles originally claimed is taught as equivalent to a predetermined number of serial data bits now claimed. Accordingly, this rejection should be withdrawn.

The application provides adequate teaching for the "predetermined number" recited in claim 4. Claim 4 recites transmission of data from the selected module as taught in the application at page 19, line 18 to page 20, line 2. This portion of the disclosure omits specific recitation of transmission of the equivalent of first section 121 illustrated in Figure 7. However, the application states at page 5, lines 16 to 18 and at lines 15 and 16 of the original ABSTRACT that this transmission from the selected module uses "the same format." The application states at page 19, lines 19 and 19 that this transmission from the selected module uses this alternate data transfer protocol." This language references the format illustrated in Figure 7 and described in the original application at page 18, lines 17 to 30, which includes first section 121 "of plural bits of the same digital state." This is adequate description of the subject matter recited in claim 4. Accordingly, this rejection should be withdrawn.

The currently employed terms "serial scan path mode signal," "alternative data mode signal" and "bypass path mode signal" are adequately taught in the application at page 19, lines 3 to 10. This portion of the original specification clearly discloses the three modes recited in claims 6 and 8. The above quoted passage further clearly states that both input switch 201 and output switch 202 select one of the three paths corresponding to a mode input. Claim 6 has been amended to change "normal mode signal" to "serial scan path mode signal" and "alternative data mode signal" to "alternate data transfer protocol mode signal" to correspond more closely to the language used in the application at page 19. This is believed within the scope of the disclosure and more informative

than "first mode" and "second mode," which the Applicant submits would be proper. Claim 8 recites "bypass path mode signal" which closely matches the above quoted language. The Applicant respectfully submits that the disclosure that input switch 201 and output switch 202 are responsive to a mode input and disclosure of the respective modes permits the Application to recite corresponding mode names in the claims. Accordingly, this objection should be withdrawn.

The Applicant respectfully submits that the original application adequately disclosed the limitation "said start bit generator generating a serial signal having a predetermined number of bits, each bit of said serial signal having a first digital state" as recited in claim 12. Claim 12 recites transmission of data from the selected module as taught in the application at page 19, line 18 to page 20, line 2. This portion of the disclosure omits specific recitation of transmission of the equivalent of first section 121 illustrated in Figure 7. However, the application states at page 5, lines 16 to 18 and at lines 15 and 16 of the original ABSTRACT that this transmission from the selected module uses "the same format." The application states at page 19, lines 19 and 19 that this transmission from the selected module uses this alternate data transfer protocol." This language references the format illustrated in Figure 7 and described in the original application at page 18, lines 17 to 30, which includes first section 121 "of plural bits of the same digital state." This is adequate description of the subject matter recited in claim 12 Accordingly, this rejection should be withdrawn.

Claims 1 to 12 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not properly described in the specification. The OFFICE ACTION notes the following inadequately disclosed subject matter. The application states at lines 19-20, page 18 "This data transfer protocol

includes a first section 121 of plural bits of the same digital state". The OFFICE ACTION states that the specification fails to disclose how to determine those plural bits (paragraph 7-1). Accordingly, without undue experiment, it is unclear how one skilled in the art may make and/or use the invention. Claim 4 recites the limitation "at said selected module, supplying a serial signal having said first logic state to following registers in the serial connection of the plurality of registers." The OFFICE ACTION questions how one skilled in the art may without undue experimentation "at said selected module" supply a serial signal to following registers because claim 1, lines 8 and 9 states that "nonselected modules being nonresponsive to data on said serial connection" (paragraph 7-2).

The Applicant respectfully submits that determining the predetermined number of bits of the first digital state does not require undue experimentation. Claim 1 recites "supplying to the test data input port for communication to the boundary-scan architecture a serial signal having a number of bits greater in number than a number of bits of the serial connection of the plurality of registers." The number of bits of the serial connection of the plurality of registers results from the product design and is presumably known to anyone who would construct a product using this invention. Regarding claim 6 which does not so limit the number of bits, one skilled in the art would realize that it is necessary to produce a number of these bits sufficient for the serial data stream to reach the selected module. The dimensions of the serial chain are presumable known and thus this predetermined number is easily determined. Note that selecting this predetermined number of bits is no different than selecting the length of the prefix 110 illustrated in Figure 6 and described in the application at page 17, line 23 to page 18, line 10. The Applicant respectfully submits that one skilled in the art would

realize the predetermined number of bits must be at least as great as the length of the known prefix 110. Thus undue experimentation is not required to determine this predetermined number. Accordingly, this rejection should be withdrawn.

The Applicant respectfully submits that the two limitations noted with regard to claim 4 are not contrary. The recitation in claim 1 that nonselected modules are "nonresponsive to data on said serial connection" does not prohibit transmission of data through the nonselected modules via the "serial connection of a plurality of registers disposed in a plurality of modules." The "following registers" recited in claim 4 do not need to be responsive to the data to transfer this data via the serial chain recited in claim 1. Note that the preferred embodiment of this invention described at page 8, line 24 to page 9, line 26 uses a protocol called IEEE 1149.1 or JTAG. In accordance with this known protocol data may be shifted into or out of the device under test via the serial stream while the device is insensitive to this data. Then the device may be placed in a normal operating mode in which it responds to the data contained in the registers forming the serial chain. The operation of the nonselected modules during the output function recited in claim 4 is no different than the scan in/scan out operation according to the prior art. Accordingly, this rejection should be withdrawn.

Claims 1 to 12 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The OFFICE ACTION notes: the limitation "logic state" is vague and indefinite because only "digital state" has been clearly defined (paragraph 9-1); and confusion within claim 6 regarding the recitation of "said serial input," "said serial data input" and "said serial data output."

Claims 1, 4 to 7 and 12 have been amended to change "logic state" to "digital state." By these amendments the recitation of these claims correspond to the teaching of the application.

Claim 6 has been amended to change both "serial input" and "serial data input" to "start bit detector input" and to change both "serial output" and "serial data output" to "start bit detector output." The Applicant respectfully submits these amendments cure any indefiniteness in claim 6.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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